CLAIMS:

1. A semiconductor device comprising:

a semiconductor substrate having an insulating surface;

a conductive pattern disposed on the insulating surface of said semiconductor substrate, said conductive pattern including at least one layer of metal or metal silicide;

a first insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said conductive pattern; and

a second insulating film made of silicon nitride formed to continuously cover said conductive pattern and said first insulating film.

2. A semiconductor device according to claim 1, wherein said first insulating film covers the side wall and upper surface of said conductive pattern.

3. A semiconductor device according to claim 2, wherein said first insulating film on the side wall of said conductive pattern is a different film from said first insulating film on the upper surface of said conductive pattern.

4. A semiconductor device according to claim 1, wherein said first insulating film extends under a bottom end of said second insulating film positioned on the side wall of said

conductive pattern.

5. A semiconductor device according to claim 1, wherein said conductive pattern is a gate electrode of a MIS transistor.

6. A semiconductor device according to claim 1, wherein said first insulating film is made of a silicon oxide film.

7. A semiconductor device according to claim 2, wherein said first insulating film is thicker at the upper surface of said conductive pattern than at the side wall thereof.

8. A semiconductor device according to claim 1, further comprising:

a third insulating film having etching characteristics different from a silicon nitride film and formed on said second insulating film made of a silicon nitride film; and

a contact area formed in said third insulating film, having a bottom portion at least partially defined by said second insulating film.

9. A semiconductor device according to claim 8, wherein the surface of said third insulating film is generally parallel to said semiconductor substrate.

10. A semiconductor device according to claim 8, further

comprising:

a conductive plug filling the contact area.

11. A semiconductor device according to claim 10, further comprising:

a fourth insulating film formed on the third insulating film and defining a contact area on said conductive plug.

12. A semiconductor device according to claim 11, further comprising:

an upper conductive pattern formed on said fourth insulating film and on said conductive plug;

a fifth insulating film made of an insulating material other than silicon nitride, and formed to cover at least a side wall of said upper conductive pattern; and

a sixth insulating film made of silicon nitride and formed to continuously cover said upper conductive pattern and said fifth insulating film.

13. A semiconductor device according to claim 12, further comprising:

another contact area formed in said third insulating film on an opposite side of said conductive pattern to said contact area, having a bottom portion at least partially defined by said second insulating film; and

another conductive plug filling said another contact area;

wherein said fourth insulating film further defines another contact area on said another conductive plug.

14. A semiconductor device according to claim 13, further comprising a storage capacitor formed on said another conductive plug.

15. A semiconductor device according to claim 14, wherein said storage capacitor is formed to at least partially cover said sixth insulating film.

16. A semiconductor device according to claim 12, further comprising:

seventh insulating film made of silicon nitride, formed between said third and fourth insulating films, and cooperatively defining said contact area with said third insulating film.

17. A semiconductor device according to claim 12, further comprising:

a field insulating film formed on a surface of said semiconductor substrate, and having a surface at a higher level than said insulating surface of said substrate;

wiring patterns formed on said field insulating film

and on said fourth insulating film; and

silicon nitride layers covering said wiring patterns.

18. A semiconductor device according to claim 17, further comprising:

an interlayer insulating layer covering said fourth insulating layer, said storage capacitor, and said silicon nitride layer covering the wiring pattern on said fourth insulating film;

connection holes formed through said interlayer insulating layer and reaching said wiring patterns; and

upper wiring patterns filling said connection holes.

19. A semiconductor device according to claim 18, wherein said storage capacitor includes a storage electrode connected to said another conductive plug, a dielectric film formed on said storage electrode and on said fourth insulating film, and an opposing electrode formed on said dielectric film and having an extension on said fourth insulating film, one of said connection holes penetrates through said opposing electrode at said extension, and one of said upper wiring patterns makes electrical contact with said opposing electrode at its side wall.

20. A semiconductor device comprising:

a plurality of first conductive layers disposed on a

substrate generally in parallel;

a first insulating film formed on said first conductive layers;

a second insulating film made of a silicon nitride film and formed on said first insulating film;

a first contact area formed in and through said first and second insulating films between said plurality of first conductive layers;

a second conductive layer formed in said first contact area;

a third insulating film having etching characteristics different from a silicon nitride film and formed on said second insulating film;

a second contact area formed in said third insulating film at the position over said second conductive layer; and

a third conductive layer connected to said second conductive layer via said second contact area.

21. A semiconductor device according to claim 20, wherein said second contact area extends to an area over said second insulating film formed at the outside of said second conductive layer.

22. A semiconductor device according to claim 20, further comprising a fourth insulating film made of a silicon nitride film, formed on said third conductive film, and having a

thickness larger than that of said second insulating film.

23. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film formed on said semiconductor substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and drain of said MIS transistor formed in said semiconductor substrate on both sides of said gate electrode;

a first insulating film formed on said semiconductor substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a second insulating film of a silicon nitride film formed on said first insulating film;

first and second contact areas formed in and through said first and second insulating films and respectively reaching said first and second impurity diffusion regions;

first and second conductive layers formed in said first and second contact areas and connected to said first and second impurity diffusion regions, respectively;

a third insulating film formed on said second insulating film;

a third contact area formed through said third

insulating film and reaching said first conductive layer; and

a third conductive layer connected to said first conductive layer via said third contact area.

24. A semiconductor device according to claim 23, further comprising:

a fourth contact area formed through said third insulating film and reaching said second conductive layer;

a fourth conductive layer constituting a storage electrode connected to said second conductive layer via said fourth contact area; and

a fifth conductive layer constituting an opposing electrode formed to face said fourth conductive layer, with a capacitor insulating film being interposed between said fourth and fifth conductive layers.

25. A semiconductor device according to claim 24, wherein said fourth conductive layer has a bottom portion and a cylindrical portion vertical to said semiconductor substrate.

26. A semiconductor device according to claim 23, wherein said third contact area extends to an area over said second insulating film formed at the outside of said first conductive layer.

27. A semiconductor device according to claim 24, wherein

said fourth contact area extends to an area over said second insulating film formed at the outside of said second conductive layer.

28. A semiconductor device according to claim 24, wherein part of the bottom portion of said fourth conductive layer is in contact with an upper portion of said second insulating film.

29. A semiconductor device according to claim 24, wherein the end portion of said fifth conductive layer and the end portion of said second insulating film are registered in a plan view.

30. A semiconductor device according to claim 23, further comprising a fourth insulating film made of a silicon nitride film and formed on said third conductive layer, wherein said fourth insulating film is thicker than said second insulating film.

31. A semiconductor device comprising:

a semiconductor substrate;

a gate insulating film formed on said semiconductor substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

impurity diffusion regions constituting a source and a

drain of said MIS transistor formed in said semiconductor substrate on both sides of the gate electrode;

a first insulating film formed on said semiconductor substrate inclusive of said gate electrode and said impurity diffusion regions;

a first contact area formed through said first insulating film and reaching at least one of said impurity diffusion regions;

a first conductive layer formed in said first contact area and connected to one of said impurity diffusion regions;

a second insulating film formed on said first insulating film;

a third insulating film of a silicon nitride film formed on said second insulating film;

a second contact area formed in and through said second and third insulating films and reaching said first conductive layer;

a second conductive layer constituting a storage electrode connected to said first conductive layer via said second contact area, said second conductive layer having a bottom portion and a cylindrical portion vertical to said semiconductor substrate; and

a third conductive layer facing said second conductive layer with a capacitor insulating film being interposed therebetween, part of said third conductive layer being in contact with the surface of said third insulating film via the

capacitor insulating film.

32. A semiconductor device according to claim 31, wherein the end portion of said third conductive layer and the end portion of said third insulating film are registered in a plan view.

33. A semiconductor device comprising:

a semiconductor substrate having a surface;

first and second conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first and second conductive layers;

a first insulating film formed on said substrate, covering said first and second conductive layers;

a first contact area formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact area formed in and through said first insulating film and said second conductive layer, said second conductive layer having a side wall exposed in said second contact area; and

a pair of third conductive layers formed at least in said first and second contact areas and connected via said first contact area to the surface of said first conduction layer and to the side wall of said second conductive layer via said second

contact area,

wherein D1 is larger than D2, where D1 is a depth from the surface of said first insulating film to said first conductive layer and D2 is a depth from the surface of said first insulating film to said second conductive layer.

34. A semiconductor device according to claim 33, further comprising a second insulating film formed under said second conductive layer and having etching characteristics different from said first insulating film.

35. A semiconductor device according to claim 34, wherein said second contact area is formed through said first insulating film, said second conductive layer, and said second insulating film.

36. A semiconductor device according to claim 34, wherein said second insulating film is a silicon nitride film.

37. A semiconductor device according to claim 33, wherein the surface of said first insulating film is planarized to be generally parallel to said substrate.

38. A semiconductor device according to claim 33, wherein said second conductive layer is a capacitor opposing electrode of a capacitor.

39. A semiconductor device comprising:

a semiconductor substrate having a surface;

first to third conductive layers formed at levels different in distance from the substrate surface, the levels becoming higher in the order of the first, third, and second conductive layers;

a first insulating film formed on said substrate inclusive of said first to third conductive layers;

a second insulating film formed under said second conductive layer and having etching characteristic different from said first insulating film.

a third insulating film formed to cover said third conductive layer and having etching characteristics same as said second insulating film;

a first contact area formed through said first insulating film and exposing the top surface of said first conductive layer;

a second contact area formed through said first insulating film, said second conductive layer, and said second insulating film, said second conductive layer having a side wall exposed in said second contact area;

a third contact area formed through said first and third insulating films and exposing the surface of said third conductive layer; and

three fourth conductive layers respectively connected to the surface of said first conductive layer via said first

contact area, to the side wall of said second conductive layer via said second contact area, and to the surface of said third conductive layer via said third contact area,

wherein D1 > D3 > D2, where D1 is a depth from the surface of said first insulating film to said first conductive layer, D2 is a depth from the surface of said first insulating film to said second conductive layer, and D3 is a depth from the surface of said first insulating film to said third conductive layer.

40. A semiconductor device according to claim 39, wherein said second and third insulating films are made of a silicon nitride film.

41. A semiconductor device according to claim 39, wherein the surface of said first insulating film is planarized to be generally parallel to said substrate.

42. A semiconductor device according to claim 39, wherein said second conductive layer is a capacitor opposing electrode of a capacitor.

43. A semiconductor device comprising:

a semiconductor substrate having a surface;

a plurality of first conductive layers formed on the surface of said semiconductor substrate generally in parallel;

first insulating films formed to cover said first conductive layers;

a second insulating film embedded between adjacent ones of said first conductive layers, said second insulating film having a surface coincident with the upper surface of said first insulating films and parallel to the surface of said semiconductor substrate; and

a contact area formed in said second insulating film, part of said contact area riding upon one of said first insulating films.

44. A semiconductor device according to claim 43, wherein said first conductive layers form a DRAM bit lines.

45. A semiconductor device comprising:

a semiconductor substrate having a surface;

a plurality of first conductive layers formed on the surface of said semiconductor substrate generally in parallel and having a plurality of levels different in distance from the surface of said semiconductor substrate;

first insulating films formed to cover said first conductive layers; and

a second insulating film embedded between adjacent ones of said first conductive layers and having a surface coincident with the upper surface of said first insulating films with the highest level in distance from the surface of said

first insulating film and parallel to the surface of said semiconductor substrate.

46. A semiconductor device according to claim 45, further comprising a contact area formed in said second insulating film, part of said contact area extending to an area over one of said first insulating films.

47. A semiconductor device according to claim 45, wherein said first insulating films are each made of a silicon nitride film.

48. A semiconductor device according to claim 45, wherein said semiconductor substrate includes a field insulating film defining active regions, said first conductive layers with the highest level in distance from the surface of said semiconductor substrate are formed on the field insulating film, and said first conductive layers with the lowest level in distance from the surface of said semiconductor substrate are formed on the active regions.

49. A semiconductor device according to claim 48, wherein said first conductive layer is a DRAM word line.

50. A semiconductor device comprising:

a silicon substrate having a surface;

a gate insulating film formed on said silicon substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and drain of said MIS transistor formed in said silicon substrate on both sides of said gate electrode;

an insulating film formed on said silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact areas formed in and through said insulating film and reaching said first and second impurity diffusion regions;

first and second conductive layers made from the same conductive layer and connected to said first and second impurity diffusion regions via said contact area;

a bit line connected to said first impurity diffusion area via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer,

wherein the impurity concentration of said second impurity diffusion region is larger than the impurity concentration of said first impurity diffusion region.

51. A semiconductor device comprising:

a silicon substrate having a surface;

a gate insulating film formed on said silicon substrate;

a gate electrode of a MIS transistor formed on said gate insulating film;

first and second impurity diffusion regions constituting source and drain of said MIS transistor, having the same impurity concentration and formed in said silicon substrate on both sides of said gate electrode;

an insulating film formed on said silicon substrate inclusive of said gate electrode and said first and second impurity diffusion regions;

a pair of contact areas formed through said insulating film and reaching said first and second impurity diffusion regions;

a third impurity diffusion region of the same conductivity type as said second impurity diffusion region formed in said silicon substrate under said contact area merging with said second impurity diffusion region, the impurity concentration of said third impurity diffusion region is larger than the impurity concentrations of said first and second impurity diffusion regions;

a first conductive layer connected to said first impurity diffusion area via one of said contact areas;

a second conductivity layer made from the same conductive layer as said first conductive layer and connected to said second impurity diffusion region and said third impurity

diffusion region via the other of said contact areas;

a bit line connected to said first impurity diffusion region via said first conductive layer; and

a capacitor storage electrode connected to said second impurity diffusion region via said second conductive layer.

52. A method of manufacturing a semiconductor device comprising the steps of:

forming a conductive layer including at least one layer of metal silicide on a semiconductor substrate;

depositing a first silicon nitride film on said conductive layer to form a lamination;

patterning said lamination;

forming an oxide film on a side wall of said conductive layer by thermal oxidation;

forming a second silicon nitride film on said semiconductor substrate including said patterned lamination and said oxide film on the side wall; and

anisotropically etching said second silicon nitride film to form a side spacer of the second silicon nitride on the side wall of said lamination inclusive of said oxide film on the side wall.

53. A manufacture method comprising the steps of:

forming a gate insulating film and a first conductive layer on a semiconductor substrate;

patterning said first conductive layer to form gate electrodes;

forming impurity diffusion regions constituting source and drain regions in said semiconductor substrate by using said gate electrodes as a mask;

forming a first insulating film on said semiconductor substrate inclusive of said gate electrodes;

forming a second insulating film made of a silicon nitride film on said first insulating film;

selectively and sequentially etching said first and second insulating films to form first contact areas reaching at least ones of said impurity diffusion regions;

forming second conductive layers in said first contact areas;

forming a third insulating film on said second insulating film inclusive of said second conductive layers;

forming a second contact area through said third insulating film, exposing one of said second conductive layers; and

forming third conductive layers connected to said second conductive layers via said second contact areas.

54. A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming on a semiconductor substrate a first conductive layer, a first insulating film, a second

insulating film made of silicon nitride, and a third insulating film;

forming a contact area reaching said first conductive layer by sequentially etching said third, second, and first insulating films;

selectively forming a second conductive film on the bottom and side wall of said contact area;

removing said third insulating film by using said second conductive layer as a mask and said second insulating film as an etching stopper to expose said second conductive layer of cylindrical shape;

forming a fourth insulating film on the surface of said second conductive film;

forming a third conductive layer on said semiconductor substrate inclusive of said fourth insulating film; and

selectively removing said third conductive layer leaving at least part of an area inclusive of said second conductive layer.

55. A manufacture method comprising the steps of:

forming a gate insulating film and a first conductive layer on a semiconductor substrate, and patterning said first conductive layer to form a gate electrode;

forming impurity diffusion regions constituting a source and a drain in said semiconductor substrate by using said gate electrode as a mask;

forming a first insulating film on said semiconductor substrate inclusive of said gate electrode;

selectively etching said first insulating film to form first contact areas reaching said impurity diffusion regions;

forming second conductive layers in said first contact areas;

forming a second insulating film on said first insulating film inclusive of said second conductive layers;

forming a second contact area through said second insulating film to expose one of said second conductive layers;

forming a third conductive layer connected to said one of the second conductive layers via said second contact area;

sequentially forming on said semiconductor substrate inclusive of said third conductive layer a third insulating film, a fourth insulating film made of silicon nitride, and a fifth insulating film;

selectively removing said fifth, fourth, third, and second insulating films over the other of said second conductive layer where said third conductive layer is not formed, to form a third contact area reaching the other of said second conductive layer;

selectively forming a fourth conductive layer on the bottom and side wall of said third contact area;

removing said fifth insulating film by using said fourth conductive layer as a mask and said fourth insulating film as an etching stopper to expose said fourth conductive

layer of cylinderical shape;

forming a sixth insulating film on the surface of said fourth conductive layer;

forming a fifth conductive layer on said semiconductor substrate inclusive of said sixth insulating film; and

selectively removing said fifth conductive layer leaving at least part of an area inclusive of said fourth conductive layer.

56. A method of manufacturing a semiconductor device comprising the steps of:

forming first conductive layers on a semiconductor substrate;

forming a first insulating film on said first conductive layers;

forming second conductive layers on said first insulating film;

forming a second insulating film on said semiconductor substrate inclusive of said second conductive layers;

forming a mask on said second insulating film for forming contact areas; and

sequentially etching said second and first insulating films by using said mask to form a contact area over said first conductive layer and sequentially etching said second insulating film and second conductive layer by using said mask to form a contact area through said second conductive layer.

57. A method of manufacturing a semiconductor device comprising the steps of:

forming first conductive layers on a semiconductor substrate;

sequentially forming a first insulating film and a second insulating film made of a silicon nitride film on said first conductive layers;

forming a second conductive layer on said second insulating film;

selectively removing said second insulating film at least at an area of a contact portion of one of said first conductive layers;

forming a third insulating film on said second insulating film, said first insulating film, and said semiconductor substrate inclusive of said second conductive layer;

forming a mask on said third insulating film for forming contact areas;

sequentially etching said third and first insulating films by using said mask to form a contact area over said first conductive layer; and

sequentially etching said third insulating film and second conductive layer by using said mask to form a contact area penetrating through said second conductive layer.

58. A method of manufacturing a semiconductor device

comprising:

forming first conductive layers on a semiconductor substrate;

forming a first insulating film on said first conductive layers;

forming a lamination of a second conductive layer and a second insulating film made of a silicon nitride film stacked on said second conductive layer, on said first insulating film;

forming a third insulating film and a fourth insulating film made of a silicon nitride film, on said semiconductor substrate inclusive of said lamination and said first insulating film;

forming a third conductive layer on said fourth insulating film;

selectively removing said fourth insulating film at least at an area of a contact portion of one of said first and second conductive layers;

forming a fifth insulating film on said semiconductor substrate inclusive of said fourth and third insulating films and said third conductive layer;

forming a mask on said fifth insulating film for forming contact areas; and

sequentially etching said fifth, third, and first insulating films by using said mask to form a contact area over said one of the first conductive layers, sequentially etching said fifth, third, and second insulating films by using said

mask to form a contact area over said second conductive layer, and sequentially etching said fifth insulating film, said third conductive layer, and said fourth insulating film by using said mask to form a contact area through said second conductive layer.

59. A method of manufacturing a semiconductor device comprising the steps of:

sequentially forming a first conductive layer and a first insulating film on a semiconductor substrate;

patterning a lamination of said first insulating film and said first conductive layer into lamination units disposed generally parallel;

forming a second insulating film on said semiconductor substrate inclusive of said lamination units and anisotropically etching said lamination units to form side spacers on side walls of said lamination units;

forming a third insulating film on said semiconductor substrate inclusive of said first conductive layer covered with said first and second insulating films;

planarizing said third insulating film by chemical mechanical polishing (CMP) by using said first insulating film as a stopper; and

partially removing said third insulating film to form a contact area, part of the bottom of said contact area extending at least over part of said second insulating film.

60. A method of manufacturing a semiconductor device comprising the steps of:

forming an element isolating insulating film on a semiconductor substrate to define an active region;

sequentially forming a first conductive layer and a first insulating layer on said semiconductor substrate inclusive of said element isolating insulating film and the active region;

patterning a lamination of said first insulating film and said first conductive layer into lamination units disposed generally parallel;

forming a second insulating film on said semiconductor substrate inclusive of said lamination units and anisotropically etching said lamination units to form side spacers on side walls of said lamination units;

forming a third insulating film on said semiconductor substrate inclusive of said first conductive layer covered with said first and second insulating films and said element isolating insulating film; and

planarizing said third insulating film by chemical mechanical polishing (CMP) by using said first insulating film on said element separation insulating film as a stopper.

61. A method of manufacturing a semiconductor device comprising the steps of:

forming a gate oxide film and a gate electrode on a semiconductor substrate of a first conductivity type;

implanting first impurity ions of a second conductivity type opposite to the first conductivity type into said semiconductor substrate by using said gate electrode as a mask to form first and second impurity diffusion regions constituting source/drain regions;

forming an insulating film on said semiconductor substrate covering said gate electrode;

partially etching said insulating film to form a first contact area reaching said first impurity diffusion region and a second contact area reaching said second impurity diffusion region;

covering said second contact area with a mask pattern;

implanting second impurity ions of the second conductivity type into said first impurity diffusion region exposed in said first contact area by using said mask pattern and said insulating film as a mask to form a third impurity diffusion region;

forming a first conductive layer connected to said third and first impurity diffusion regions via said first contact area and a second conductive layer connected to said second impurity diffusion region via said second contact area;

forming a DRAM storage electrode connected to said third and first impurity diffusion regions via said first conductive layer; and

forming a DRAM bit line connected to said second impurity diffusion regions via said second conductive layer.